Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor device structure formed on a substrate defining a substantially horizontal plane, the semiconductor device structure comprising:

~~a substrate defining a substantially horizontal plane;~~

a source region;

a drain region;

a gate electrode disposed on [[said]] the substrate and [[being]] electrically insulated ~~therefrom~~ from the substrate, said gate electrode positioned vertically between said source region and said drain region; and

a plurality of semiconducting nanotubes, each of said semiconducting nanotubes including a first end electrically coupled with said source region, a second end electrically coupled with said drain region, and a channel region extending vertically through said gate electrode between said source region and said drain region, said channel region being electrically insulated from said gate electrode, and said gate electrode configured to receive a control voltage effective to regulate current flow through said channel region of ~~a respective one~~ each of said semiconducting nanotubes between said source region and said drain region.

2. (Previously Presented) The semiconductor device structure of claim 1 wherein said source is composed of a catalyst material effective for growing said semiconducting nanotubes.

3. (Previously Presented) The semiconductor device structure of claim 1 wherein said drain is composed of a catalyst material effective for growing said semiconducting nanotubes.

4. (Previously Presented) The semiconductor device structure of claim 1 further comprising:

an insulating layer disposed between said drain and said gate electrode for electrically isolating said drain from said gate electrode.

5. (Previously Presented) The semiconductor device structure of claim 1 further comprising:

an insulating layer disposed between said source and said gate electrode for electrically isolating said source from said gate electrode.

6. (Currently Amended) The semiconductor device structure of claim 1 wherein said ~~at least one~~ semiconducting ~~nanotube is~~ nanotubes are composed of arranged carbon atoms.

7. (Cancelled)

8. (Currently Amended) The semiconductor device structure of claim 1 wherein said ~~at least one~~ semiconducting ~~nanotube is~~ nanotubes are oriented substantially perpendicular to said horizontal plane.

9-24. (Cancelled)

25. (Currently Amended) A semiconductor device structure formed on a substrate, the semiconductor device structure comprising:

~~a substrate;~~

an electrically-conductive first plate on [[said]] the substrate;

an electrically-conductive second plate disposed vertically above said first plate;

an electrically-conductive layer disposed between said first and second plates;

a plurality of nanotubes, each of said nanotubes having [[an]] a first end electrically coupled with said first plate for increasing an effective area of said first plate and a second end, and each of said nanotubes ~~positioned in~~ extending vertically through said electrically-conductive layer from said first end to said second end; and

a plurality of dielectric ~~layer coating said length of each of said nanotubes such that~~ layers,

wherein each of said nanotubes [[are]] is electrically isolated from said electrically-conductive layer by a first portion of a respective one of said dielectric layers and ~~said nanotubes are~~ is electrically isolated from said second plate by a second portion of the respective one of said dielectric layers.

26. (Currently Amended) The semiconductor device structure of claim 25 wherein said ~~at least one nanotube has~~ nanotubes have a conducting molecular structure.

27. (Currently Amended) The semiconductor device structure of claim 25 wherein said ~~at least one nanotube has~~ nanotubes have a semiconducting molecular structure.

28. (Currently Amended) The semiconductor device structure of claim 25 wherein each of said dielectric [[layer]] layers comprises a shell that encases a respective one of said ~~at least one nanotube~~ nanotubes with the proviso that said first end that is electrically coupled with said first plate.

29-33. (Cancelled)

34. (New) The semiconductor device structure of claim 25 further comprising:

a plurality of gate dielectric layers, said channel region of each of said semiconducting nanotubes electrically isolated from said gate electrode by a respective one of said gate dielectric layers.